**LAB 1 REPORT: DATAPATH AND INSTRUCTION DECODER FOR RISC-V**

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**Introduction**

The primary goal of this lab was to design the datapath and instruction decoder for a simplified RISC-V core using VHDL. The design supports Register-Register, Register-Immediate, Jump, and branch instructions, with load/store operations managed separately. The implementation was verified through simulation waveforms, and I added error-handling code to each test bench to ensure the correct functionality of the datapath.

**Design Overview**

The datapath was designed according to the specifications outlined in the Lab1 manual. The main components are:

* Register File (register.vhd): It stores and provides operands via ports A and B, and supports writing to a destination register when Dlen = 1.
* ALU (alu.vhd): performs arithmetic and logical operations based on the ALUFunc signal. Inputs are selected through Asel/Bsel and multiplexed with PCout or IMM, respectively, according to PCAsel and IMMBsel.
* Program Counter (PC) (PC.vhd): It manages instruction sequencing by incrementing by 4 when the PCie is “1”. It also directly loads a new value from the ALU output, used for branch and jump targets. The load enable input to the PC is driven by the logical OR of the branch control output (isBR and BRcond) and PCle. This ensures the PC updates either for sequential execution or when a branch or jump condition is satisfied.
* Branch Unite(branch.vhd): Evaluates BRcond and asserts control signals for program counter updates when isBR = 1.
* Datapath Integration (datapath.vhd): it connects the register file, ALU, PC, and branch. Implements multiplexers and buses as specified.
* Testbench (datapath\_testbench.vhd): it provides stimuli to verify the correct behavior of datapath signals and outputs. Every test has an error-handling method, so if an error occurs, it stops and indicates where the error is happening.

The control signals are summarized and given in the lab manual.

A screenshot of a computer program

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*Figure 1: The control words*

A diagram of a computer

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*Figure 2: The top-level schematic of the datapath implementation. Each module (U\_REG, U\_ALU, U\_BRANCH, and U\_PC) is connected according to the RISC-V datapath specification. Multiplexers manage data path selection based on control signals such as PCAsel, IMMBsel, and PCDsel.*

**Simulation and Verification**

Simulation was performed using the datapath testbench code. The register write/read test verifies that Asel and Bsel select the correct register operands, and enabling Dlen writes the results to Dsel. The ALU operations confirmed outputs for arithmetic and logical functions according to ALUFunc. The PC operation verified PC interconnect (PCie = 1), direct PC loading (PCle = 1), and jump branch resolution via the branch unit. Finally, the immediate handling will verify that IMMBsel = 1 correctly feeds the immediate value into the ALU inputs.

In every code I have put error handler like the image shown below

A screenshot of a computer

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Figure 3: Error Handler codes in every test are complete.

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Figure 4: Waveform result for each test pass.

**Discussion**

The datapath was successfully designed and verified using error handler code and waveform analysis. During testing, a few implementation issues arose. One critical issue was ensuring the synchronization of register writes (Dlen) with the clock edge to avoid discrepancies between alu\_y and regA\_q. Additionally, the timing of control signals such as PCle and PCie required careful testing to confirm correct branching behavior. Although these two issues took more time to resolve, the error handler code was very helpful in confirming the results and allowed me to review everything thoroughly.